

ABSTRACT OF THE DISCLOSURE

A shift register circuit includes a first shift register having a plurality of stages connected in cascade, and a second shift register having more stages than the first shift register. The stages of the second shift register are divided into groups each formed of consecutive stages. The stages of the first shift register output pulse sequences having a predetermined number of consecutive pulses and having different phases from each other, to the stages constituting the groups of the second shift register as clock signals.

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